

Phase Current Sensor and Short-Circuit Detection based on Rogowski Coils Integrated on Gate Driver for 1.2 kV SiC MOSFET Half-Bridge Module

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Abstract—Silicon-carbide (SiC) MOSFETs are enabling electrical vehicle motor drives to meet the demands of higher power density, efficiency, and lower system cost. Hence, this paper seeks to explore the benefits that a gate-driver-level intelligence can contribute to SiC-based power inverters. The intelligence is brought by PCB-embedded Rogowski switch-current sensors (RSCS) integrated on the gate driver of a 1.2 kV, 300 A SiC MOSFET half-bridge module. They collect two MOSFET switch currents in a manner of high magnitude, high bandwidth, and solid signal isolation. The switch-current signals are used for short-circuit detection under various fault impedances, as well as for phase-current reconstruction by subtracting one switch current from another. The fundamentals and noise-immunity design of the gate driver containing the RSCS are presented in the paper and can be applied to any half-bridge power module. A three-phase inverter prototype has been built and operated in continuous PWM mode. On this setup, the performance and limitations of the short-circuit detection and phase-current reconstruction are experimentally validated by comparing with commercial current probes and Hall sensors.

Index Terms—Gate driver, Rogowski switch-current sensor, phase current reconstruction, short-circuit protection, SiC MOSFET

I. INTRODUCTION

The technology trends in power electronics applications are striving to achieve high density and high efficiency conversion. Integrating silicon carbide (SiC) power MOSFETs has become an attractive solution due to their high breakdown electric field, high working temperature, fast switching speed and low on-state resistance [1], [2], [3], and [4]. Enabled high switching frequency operation allows reduction of bulky passive components improving the power density of converters. Recent cost decrease of SiC MOSFET due to the increased usage in industry applications can result in lower overall system cost than conventional Si-based designs [5]. Therefore, SiC MOSFET presents great potential in high power applications.

When used in SiC MOSFET motor-drive inverter applications, GDs must ensure excellent performance. They must

satisfy the following requirements: isolation, sufficient driving capability (gate current) to enable fast switching of the device, high noise immunity, low propagation delay, and reliable low-level protection. The major challenges for SiC MOSFET device GDs are listed as follows:

- 1) *High noise immunity design* - due to a harsh dv/dt environment caused by the fast switching of devices, common mode (CM) noise related problems may arise, such as excessive EMI (can penetrate to the digital controllers and create electromagnetic compatibility problems in the system) and GD malfunction (logic signals may suffer resulting in unwanted PWM sequences) [6]. Therefore, special attention must be dedicated to make the GD immune to CM noise.
- 2) *Low level protection* - SiC MOSFETs output characteristics are soft in transition from linear to saturated region, and fault current can quickly rise up to values above $10xI_d^{rated}$. They can withstand these severe conditions several μs , evidencing much lower robustness than their Si IGBT counterpart due to higher current density and smaller chip area. Furthermore, new SiC MOSFET power module package tend to have low internal inductance which results in very fast SC di/dt causing possible destruction due to excessive dissipated energy. Therefore, detection time is critical for the protection of SiC MOSFETs due to the limited SC withstand time. Desaturation (DeSat) detection method (most exploited in IGBT applications) necessary blanking time, sensitivity to temperature, susceptibility to noise, the high-voltage diode and its parasitic capacitance, may render it unsuitable for SiC device protection, thus necessitating a new short-circuit protection method [7], [8].

Due to the necessity of introducing a new fast and reliable SC protection method for SiC MOSFET modules, and high-density, high-efficiency trends, PCB-embedded RSCS integrated on the GD has been researched [7], [9], and [10]. This high noise immunity, high bandwidth, and high accu-

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racy measurement resolves all problems of DeSat detection method. Since both switch currents are measured and used for protection, those pieces of information can also be used for reconstructing the phase current via simple manipulation on the GD itself. This can possibly allow increase in power density and efficiency since existing current sensing method can be eliminated such as Hall effect sensor (bulky, expensive and susceptible to external magnetic fields) and current shunts (intrusive to circuit, introduce additional loss and reduce inverter). Phase current information for continuously switched pulse-width modulation (PWM) inverters can then be sent back to the main controller for control purposes, without any additional effort from it in reconstruction, or any additional current sensing in the system.

II. GATE DRIVER ARCHITECTURE AND FUNCTIONAL CIRCUIT DESIGN

A. Phase Current Reconstruction Principle

Fig.1 shows basic configuration of the half-bridge, GD with integrated RSCS and some of the critical current waveforms. From t_0 to t_1 , the bottom switch is turned on, and the RSCS that is sensing the bottom switch current provides the voltage proportional to the current. In this instance, since the top switch is turned off, there should not be current flowing through, so the output of the top RSCS is equal to zero. In the rest of the switching cycle period (t_1 to t_2) when the top switch is on, the situation is reversed. The top RSCS provides voltage proportional to the current through the switch, while the voltage of the bottom is clamped to zero since no current is flowing through the bottom switch. By knowing each switch's current in the complete switching cycle, outputting the phase current from the GD is possible by constantly subtracting these two currents.

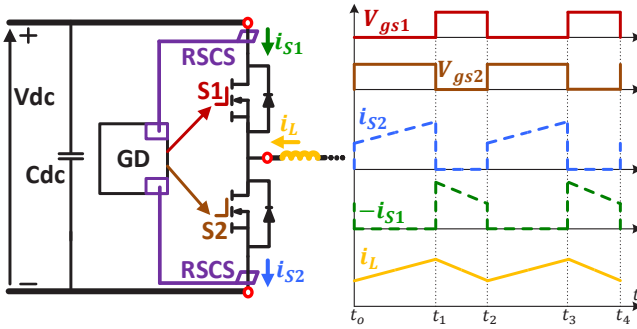


Figure 1. Phase current reconstruction principle

To obtain phase current information, measurements from RSCS-s need to be combined/subtracted on the common ground of the GD which is on the same ground as controller. Since all commercial current sensors have analog output, analog information of reconstructed current will be considered in order to emulate commercial current measurement and compare results with it. Two possibilities of reconstructing the phase current arise, analog and digital shown in Fig.2

Fig.2a) illustrates that analog reconstruction requires only a simple operational amplifier (OpAmp) with resistor network to

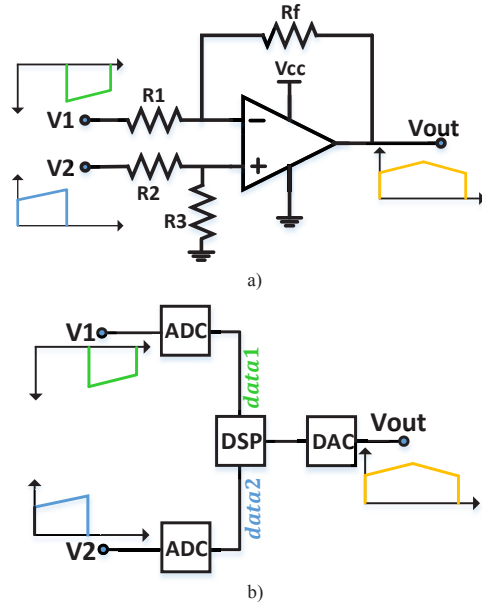


Figure 2. Phase current: a) analog reconstruction, b) digital reconstruction

obtain phase current information. If $R_1 = R_2$ and $R_3 = R_f$, then output phase current would simply be defined as in (1):

$$V_{out} = -\frac{R_f}{R_1}(V_1 - V_2) \quad (1)$$

where voltage V_1 of the top RSCS represents current through top switch and voltage V_2 mirrors bottom switch current coming from the bottom RSCS.

Fig.2b) shows the principle of digital reconstruction. In order to subtract two current information in some sort of digital-signal processor (DSP), two analog-to-digital converters (ADCs) are required. Since analog information of reconstructed current is needed, a digital-to-analog converter (DAC) is necessary to convert phase current information back to analog, which is described by (2):

$$V_{out} = -V_{ref} \frac{data2 - data1}{2^n} \quad (2)$$

where V_{ref} is the voltage reference of the DAC, and $data2$, $data1$ are the digital representations of the corresponding switches currents, and n is the bit number of the DAC.

B. Gate Driver Architecture

GD architecture types in which RSCS-s are placed on the isolated side are not considered. This is due to the complexity of transferring information (either analog or digital) over the isolation barrier for reconstruction purposes as well as possible synchronization problems. The only GD architecture types considered are ones in which RSCS-s are already on the common ground (controller ground). Based on the ways of reconstructing the phase current information, two possibilities exist: either a GD architecture type with analog reconstruction or a GD architecture type with digital reconstruction. Based

on a comprehensive analysis of advantages and drawbacks of each GD architecture type, comparison Table I is formed.

Table I
COMPARISON OF CONSIDERED ARCHITECTURE TYPES

Comparison criteria	Architecture types	
	Analog reconstruction	Digital reconstruction
Estimation of phase current delay	≈ 700 ns	≈ 1.5 μ s
Short-circuit propagation delay	50 ns	50 ns
Noise susceptibility	Fair	Fair
Part count	Fewer	More
Automatic calibration of RSCS	N\A	Possible
Improved reset timing for RSCS	N\A	Possible
Compatibility with analog and digital controller	N\A	Possible

Even though the analog-based architecture has a lower parts count and smaller phase current delay, digital reconstruction is chosen since the phase current delay of $\approx 1.5 \mu s$ is not severe for inverter stage electric vehicle applications with intended switching frequency of $30 kHz$. Moreover, digital reconstruction with a local DSP enables different possibilities such as the potential for automatic calibration of RSCS, improved reset timing for RSCS based on switch current value, and compatibility with both analog and digital controllers. The final implemented architecture is shown in Fig.3.

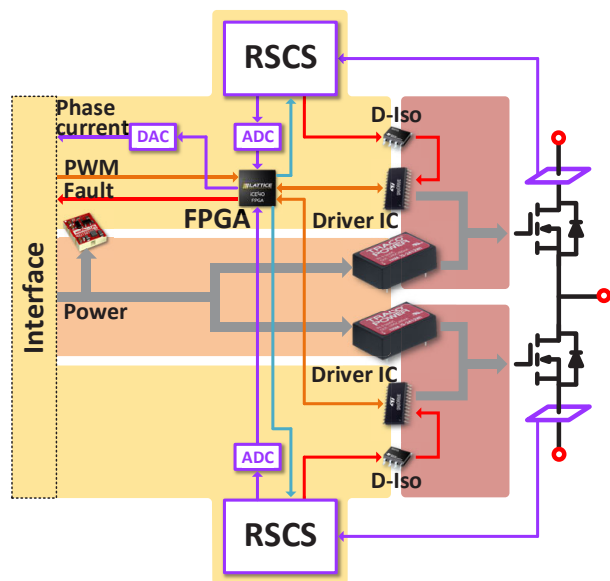


Figure 3. Gate driver architecture with digital reconstruction of the phase current where RSCS are on the controller ground

Field-programmable gate array (FPGA) is employed for digital subtraction, resetting and turning off RSCS when the corresponding switch is not conducting. An SC fault signal

is transmitted through the digital isolator to the isolated side to trigger the soft turn-off option of the GD IC. In order to strengthen the signal path in front of the common mode current, an isolated power supplies with the minimum possible parasitic capacitance are chosen. The smaller the parasitic capacitance, the less CM current will be introduced due to its larger impedance on higher frequencies. CM chokes are also employed in series with the main power supplies in order to provide high impedances at high frequencies [6]. Also, power supply traces and main power ground are put in a separate layer of PCB than the signal ground to further enhance CM noise reduction. Furthermore, split analog/digital ground plane is utilized to isolate the sensitive analog circuits from the noisy digital circuits and to reduce possibility of nuisance signals and noise induced malfunction.

C. Functional Circuit Design and Prototype

The circuit design is carried out based on that described in prior research [7], and [9]. After compressive comparison done in [9], the driver STGAP1AS demonstrates the best performance and the circuit design is based on the chosen GD IC. An under-voltage lock-out (UVLO) and over-voltage lock-out (OVLO) are employed by the GD IC so that the power supply voltage can be monitored. In case of over-current/short-circuit detection, a fault signal from the RSCS is transmitted through the digital isolator to the GD IC which will initiate soft turn-off (two-level turn off - 2LTO), and system will be shut down in a safe manner. Last but not least, Active Miller Clamping (AMC) is employed to absorb the Miller current and prevent partial shoot-through events.

As far as the PCB-embedded RSCS is concerned, since a 1.2 kV 300 A Cree module has the same package as the 1.7 kV 300 A version, the same principal and design procedure is followed as in other work reported in [10], [7], and [9]. The switch current sensor is basically composed of a Rogowski coil and an integrator. Rogowski coils are placed around one turn conductors (source of the bottom device and drain of the top device) in the 6 layer PCB. In order to increase the sensitivity of the sensor, the mutual inductance M should be as high as possible. Accordingly, 176 turns of windings have been designed after an effort to maximize the turn number. This is the maximum number that can be achieved by regular PCB fabrication techniques. The Rogowski coil serves as a differentiator that generates a di/dt value of the sensed current scaled by a factor of the mutual inductance. The signal processing-circuit is designed to integrate that information. An active integration circuit using OpAmp is selected instead of an RC passive one to achieve wider sensor bandwidth. To resolve the problem of an input offset of OpAmp being constantly integrated and invalidating the output of the sensor, a reset switch is added to the integrator to reset the output to zero when the SiC MOSFET is switched off. Eventually, the RSCS can sense pulsating current with correct amplitude and DC offset which is the current that is going through the switch. Furthermore, offset compensation circuit is implemented to minimize input offset integration error. Sensed current is then

being sent to the comparator which serves as indicator of SC. At the same time, sensed current waveform is being sent to ADC and later on to FPGA for the phase current reconstruction. Fig.4 shows the prototype GD board with RSCS and a phase current sensor.

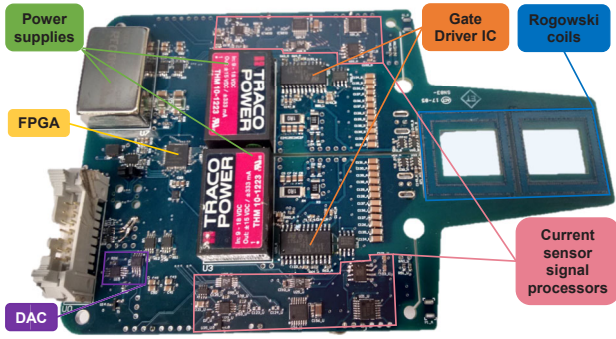


Figure 4. Prototype gate driver board with integrated current sensors

III. PHASE CURRENT RECONSTRUCTION AND SENSOR PERFORMANCE

A. Digital Reconstruction Detailed Diagram and Delay Breakdown

Fig.5 shows more detailed diagram of digital phase current reconstruction with RSCS measurement.

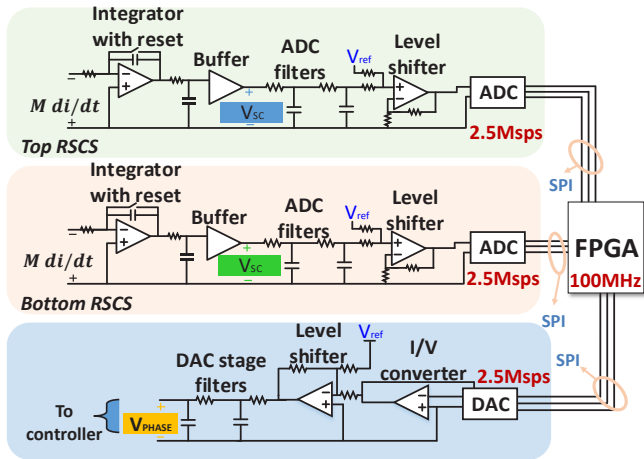


Figure 5. Detailed block diagram of digital phase current reconstruction

di/dt information, scaled with a factor of mutual inductance, is being constantly integrated by an active integrator. The output voltage of an integrator which linearly represents current in the system is filtered with the 30 MHz high frequency RC filter, to eliminate possibility of any undesirable high-frequency signals. After filter, there is buffer OpAmp. The purpose of the buffer is that any manipulation done afterward, does not interfere with the integrator circuit. After buffer, there is a two-stage ADC filter with a cutoff frequency of 3.3 MHz, the main role of which is to filter out any high frequency ringing in the current information during switching instances, thus preventing aliasing in the information. The OpAmp level shifter is employed to adjust the signal to the

proper values for ADC sampling. A high precision 14-bit ADC with ability for over 2 Msps and 50 MHz serial peripheral interface (SPI) communication clock rate is chosen. The chosen sample rate is pushed to 2.5 MHz in order to reduce delay of the current measurement. Two ADCs for top and bottom switch currents are synchronized, and they work in non-stop sampling mode in order to send sampled data in the FPGA at the same time instances. After data from ADCs is received, the FPGA performs digital subtraction of data in one clock cycle (10 ns). Immediately after successful subtraction, FPGA starts placing that information on the DAC SPI bus. A 16-bit, 2.5 Msps, 50 MHz SPI clock rate DAC with small settling time is chosen to convert information back to analog without creating a lot of additional delay. Since the DAC is a single-channel current output, an additional external I/V converter OpAmp is employed. This particular OpAmp must have a sufficiently low offset voltage such that it is not modulated by the DAC output terminal impedance change. After the I/V OpAmp there is additional level shifter to invert and adjust current information according to the controller requirements. Another two-stage RC filter with cutoff frequency of 3.3 MHz is employed to filter out the staircase waveform coming from the DAC reconstruction process. Based on the previous analysis, the phase current delay can be expected to be in the range of 1.6 μ s, which is shown in the (3):

$$\begin{aligned} t_{dly}^{PhsC} &= t_{dly}^{intg} + t_{dly}^{RC} + t_{dly}^{2stageRC} + t_{dly}^{lvlshft} + t_{dly}^{ADC} + \\ &\quad t_{dly}^{FPGA} + t_{dly}^{DAC} + t_{dly}^{lvlshft} + t_{dly}^{2stageRC} \\ &= 40ns + 30ns + 300ns + 40ns + 400ns \\ &\quad + 10ns + 400ns + 40ns + 300ns = 1.56\mu s \end{aligned} \quad (3)$$

B. Phase Current Sensor Performance

The phase current reconstruction principle will be verified on a 500 V, 300 A double-pulse test with clamped inductive load. Phase current in this case is inductor current. Results are shown in Fig.6.

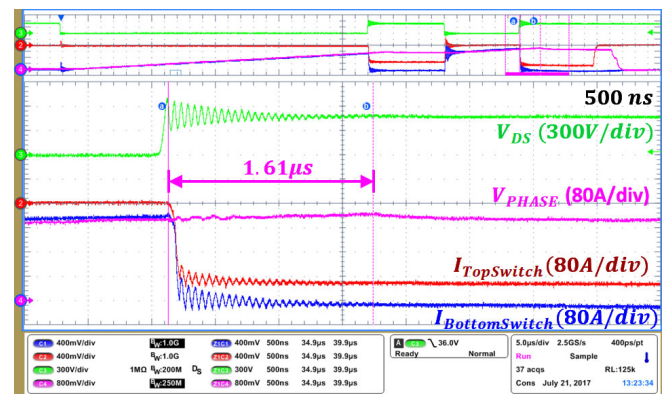


Figure 6. Double pulse test results and phase (inductor) current delay

Fig.6 clearly shows that the reconstructed phase current waveform (pink) is the result of subtracting the top switch current (red) from the bottom switch current (blue). Delay

between the reconstructed phase current and the switch current sensed with the commercial Rogowski coil probe is $1.61 \mu\text{s}$, which is approximately same as the delay estimated in Table I and the delay given in the delay breakdown analysis from previous subsection. From the reconstructed phase current waveform, no significant switching noise at the switching transients can be noticed, meaning that the employed filter values are sufficient, and a possible increase of output filter corner frequency to reduce delay, may be applied.

One of the biggest concerns in the applications where Rogowski coil measurement is being used, is the droop (drift) effect when lower frequency AC or long pulse signals are applied. The droop effect is a result of the imperfections of the OpAmp integrator circuit, where input offset error is constantly being integrated together with the incoming Mdi/dt information, resulting in a severe output voltage error over longer time periods. This being said, it is necessary to evaluate sensor performance at different switching frequencies (different lengths of on-time). A comparison is executed between RSCS and the commercial current sensor. Measurements are taken at the end of the switching interval, since that is where the droop effect is at its most intense. After that, circuit will reset or disable the output of the integrator, depending of the implementation, and drooping effect will return back to zero. Fig.7 shows the relative error of the RSCS (solid line) through the frequencies of pulse from 1 kHz to 100 kHz, for 50% on-time. Besides that, Fig.7 shows the relative error of the reconstruction process (dashed line), where reconstructed value is compared with the RSCS at the end of the switching interval. This comparison is done in order to determine how much the reconstruction process is contributing to errors, thus influencing accuracy of the phase current sensor. All measurements are taken at room temperature, since this GD is made to validate the reconstruction principle in environments with high CM noise.

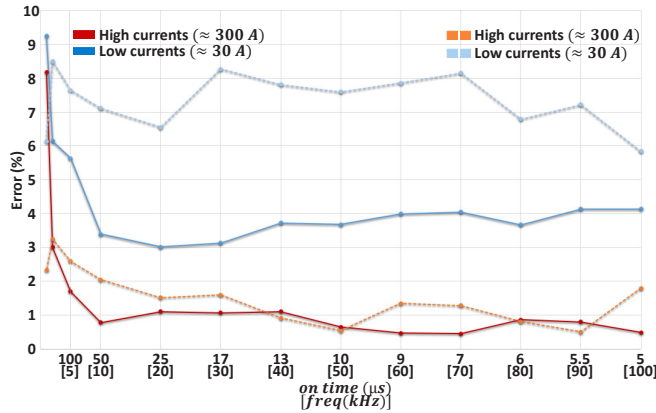


Figure 7. Error diagram of switch and phase current sensor

Fig.7 shows that high current relative error (considering RSCS comparison with commercial sensor) is low and is around 1 % for frequencies higher than 10 kHz. Absolute error, considering high current, is than a maximum of 3 A. Low current relative error is approximately 4 % for frequencies

higher than 10 kHz. Absolute error considering this case is again smaller than 3 A. However, when switching frequency is reduced below 10 kHz, relative error starts ascending enormously due to severe integration error of the integrator OpAmp for both low and high currents. The previous results turned out to be promising for power modules with intended switching frequencies above 10 kHz, which are within the SiC MOSFET domain. Reconstruction error (reconstructed phase current with respect to the output of the RSCS) ranges from 0.5–3 % for all considered switching frequencies in a high current case. Low currents have a slightly higher relative error, ranging from 6–8.4 %. Even though this relative error seems large, in absolute values it is smaller than 3 A for a 30 A current. As expected, compared reconstruction error does not depend on switching frequency.

C. Sensor Performance in Inverter Application

The experimental inverter test setup is shown in Fig.8. Three of the developed GDs with phase current sensors are connected to the 1.2 kV, 300 A SiC MOSFET modules. The inverter is mounted on the water-cooled heat sink to avoid overheating during continuous testing. Inverter DC voltage was set to be 600 V. Used source was able to provide 100 kW max, 1 kV max. The load is consisted of a 0.27 mH three phase inductor together with a water-cooled 1.7Ω resistor in each phase. Modulation used to control inverter is open loop sinusoidal PWM (SPWM), due to implementation simplicity. Modulation index is set to be around 0.9. Dead-time in this case, since turn-on and turn-off time of the switches is very fast ($<100\text{ns}$), is set to be 300 ns. The switching frequency was 30 kHz, while modulation (line) frequency was 400 Hz.

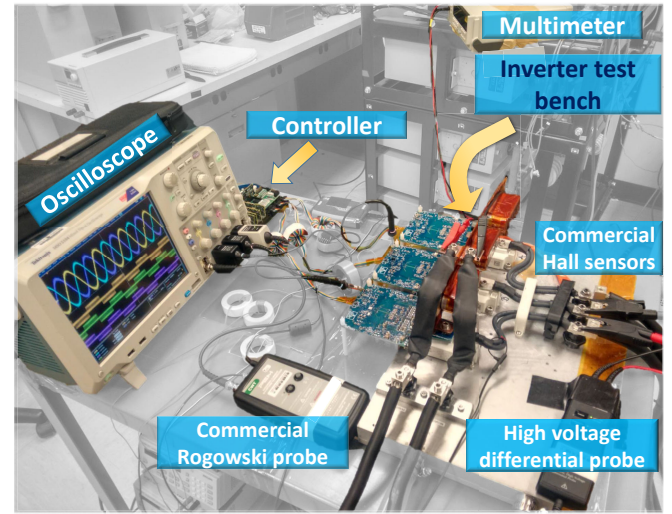


Figure 8. Three phase inverter experimental setup

Fig.9 shows the reconstructed sinusoidal current from one of the phases, together with the switches current in the corresponding phase.

As seen before in Fig.6, Fig.9 clearly shows the reconstructed phase current waveform (blue) is the result of subtracting top switch current (red) from the bottom switch current

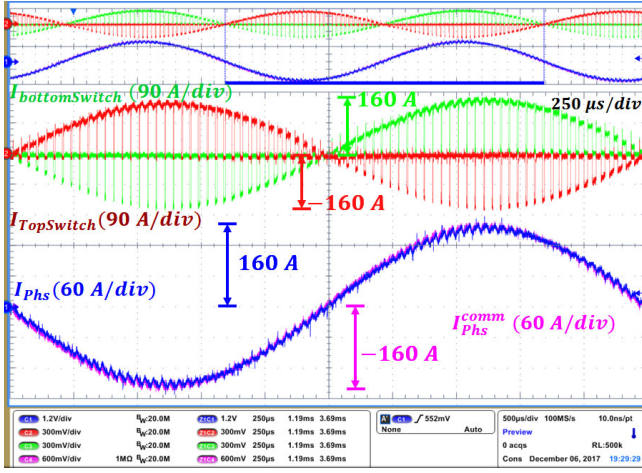


Figure 9. Reconstructed phase current of the inverter phase

(blue), now for the inverter case. The delay is still consistent and its value is $1.6 \mu\text{s}$. Besides that, a comparison with the commercial measurement (green) can also be seen in Fig.9. The reconstructed phase current follows the commercial measurement very well in both amplitude and phase with pre-determined delay. These tests are performed with the very low gate source external resistance ($R_{GS}^{on} = 0.3 \Omega$, $R_{GS}^{off} = 0.15 \Omega$) in order to push the transient speed and reduce switching losses. The dv/dt in this case was 15 V/ns , which cannot be pushed much more due to large internal gate resistance of 3Ω . In this noisy environment, the switch currents in Figure 10 show that there are no shoot-through events caused by either the Miller effect or induced signal malfunction. Furthermore, the components chosen to participate in phase current reconstruction cope well with the CM noise created by the dv/dt , and successfully reconstruct the phase current.

Since accuracy of the sensor has already been assessed in the previous subsection, linearity error (non-linearity) will now be explored as it is one of the crucial aspects of analog sensors. Due to the analog output of the phase current sensor, linearity is very important in order to have correct measurement. Even though the Rogowski coil is linear element without possibility of reaching saturation (basically air core, since FR4 is not ferromagnetic material), the integrator OpAmp, buffer stages ADC, FPGA or DAC may influence linearity and result in a non-linear transfer function between phase current and analog voltage information that represents it. The linearity error of the transducer is an expression of the extent to which the actual measured curve of a sensor departs from the ideal curve. Based on the definition given in [11], the linearity error is the maximum positive or negative discrepancy with the reference straight line (ideal curve), expressed in the full scale of measured current. That definition translates to the (4):

$$\text{Linearity error}(\%) = \frac{\Delta V(V)}{I_p^{max} \cdot G(\Omega)} \quad (4)$$

The mentioned straight line (ideal curve) is defined based

on the sensitivity of the sensor. Sensitivity of the phase current sensor is set to be (5):

$$G(\Omega) = \frac{V_{out}(V)}{I_{phs}(A)} = \frac{1.2 V}{60 A} = 0.02 \Omega \quad (5)$$

Fig.10 shows the experimental results for linearity error, where the blue line represents the ideal case reference line based on defined sensitivity. The black lines represents bounds of maximum positive and negative error.

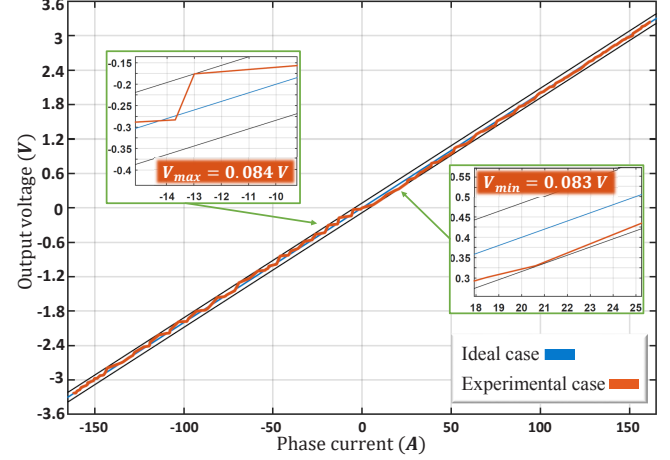


Figure 10. Linearity error of the phase current sensor

Output voltages are measured for a range of currents from $-165 \div 165 \text{ A}$, and for the reference current, a commercial Hall-effect sensor measurement is taken under the assumption that it is perfectly linear. Fig.10 shows that the maximum discrepancy of output voltage from the reference line is 0.084 V . Based on the given equation, linearity error is 2.5% . This outcome could have been somewhat expected based on the results of the accuracy measurement in previous subsection and from the performance observed in Fig.7. Linearity error is a bit larger than anticipated, however this can be significantly improved in the next versions of the GD with integrated current measurements.

IV. SHORT-CIRCUIT PROTECTION

As reported in other research [12], $1.2 \text{ kV } 300 \text{ A SiC MOSFET}$ module can reach 5 kA in less than $1.5 \mu\text{s}$ on 600V . If protection does not interrupt these extreme conditions before $3 \mu\text{s}$, the module will be destroyed due to either thermal runaway or gate breakdown. Therefore, the implemented protection needs to achieve: 1) fast detection and reaction time, which will impact the current-peak level, limiting overheating and current stresses, 2) turn-off in a safe manner, limiting the excessive overshoots created by induced voltages on parasitic inductances due to enormous di/dt during the turn-off of SC current, 3) responsiveness for all SC types and not degrade conduction or switching characteristics, 4) high noise immunity and if possible 5) inexpensiveness and easy implementation\integration in any gate driver.

A. Protection Principle

The detection and protection mechanism is shown in Fig.11.

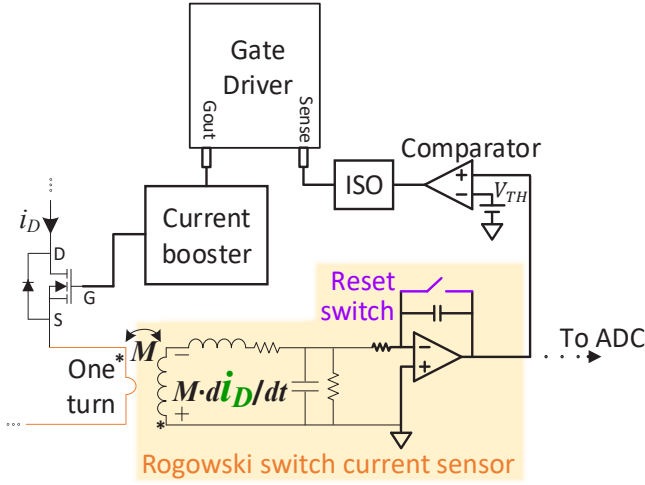


Figure 11. Detection and protection mechanism with Rogowski switch current sensor

The output voltage of the integrator OpAmp, which linearly represents high bandwidth sensed current through the switch, is sent to the comparator, which compares it with the value that is set to be an indicator of SC. The voltage source (value that indicates SC) is set to a value that corresponds to 600 A, which is the 2 times higher value than the rated one in the module. This value is chosen in order to avoid detecting SC at current peaks during the turn-on of the device, which can be up to 1.8 times rated current at both high and low temperature. Therefore, whenever there is current higher than 600 A in the system, the comparator will generate a fault signal. Fault signal is then transmitted through the digital isolator to the isolated side of GD in order to trigger the protection. The sense pin of GD IC on the isolated side is utilized to serve as an both OC and SC indicator [13]. When fault signal (logical '1') is on this pin, the driver IC will initiate soft turn-off (2LTO) after 200 ns of processing time, and the system will be shut down in a safe manner. This type of protection is limiting the excessive voltage overshoots induced on parasitic inductances due to enormous di/dt during the turn-off of SC current. Principle of operation is simple, when fault signal is brought to the sense pin, gate voltage is lowered from one driving the device in normal conditions, to lower one limiting the current in the SC event. 2LTO voltage is programmed to be 7 V, while time spent in 2LTO is programmed to be 750 ns.

B. Experimental Results

SC event and protection performance are shown on Fig.12. This particular SC event is called Fault under load (FUL) [14]. FUL is a type of fault that occurs when the device is on and conducting. The bottom device is gated on and is carrying steady current within its ratings. The fault is imposed on the system by turning on the complementary switch, thus causing the shoot-through event. Due to a very low stray

inductance in the current path, the current rise in this case is severe (FUL is considered one of the worst cases of SC as well as hard switching fault – HSF). From Fig.12 the device was conducting prior to SC for 1.6 μ s. When the SC occurs, by turning on the top switch, the current starts rising with $di/dt \approx 15$ A/ns. When the device current exceeds the threshold value of 600 A, a fault signal is generated by the comparator and is then transmitted to the sense pin (≈ 80 ns detection time). The GD IC processes that information for 100 ns, plus an additional delay time of 100ns which is the soft turn-off initiation time. This will result in a reaction time of 200 ns. After that, 2LTO is initiated and the device goes into the soft turn-off process which lasts 750 ns, with gate voltage of 7 V to limit the SC current. The maximum voltage overshoot was 270 V, and current peak 5.1 kA. Energy dissipated was: $E=0.9$ J, which is not near 6.9 J breakdown energy of this module [12]. A fast detection time of 80 ns and reaction time of 200 ns are achieved limiting overheating in the module. Besides that, the 2LTO limits excessive overshoots and put them in the range below 300 V, even though ≈ 5 kA current was interrupted.

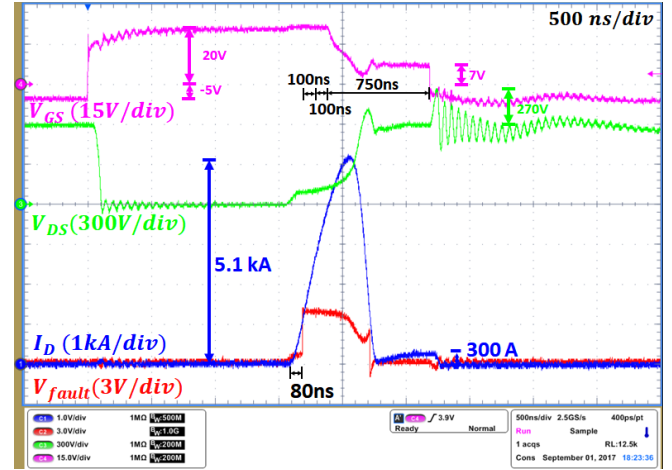


Figure 12. Short-circuit protection performance

V. CONCLUSION

The chosen GD architecture with digital phase current reconstruction is proven to perform well and is able to successfully reconstruct the phase current under a dv/dt of 15 V/ns, which in some cases creates huge amounts of CM noises. The delay between reconstructed phase current and the switch current sensed with a commercial Rogowski coil probe is 1.61 μ s, which roughly corresponds to the delay breakdown analysis. Absolute error considering RSCS for both high and low currents is a maximum of 3 A for frequencies above 10 kHz. This could be promising for power modules with intended switching frequencies above 10 kHz, and which are within the SiC MOSFET domain. Similarly, the reconstruction error is a maximum of 3 A for both high and low currents. However, there is room for improvement of these results, since better OpAmps, ADC-s, DAC and faster SPI bus speed and

sampling time could be implemented. As far as the linearity error is concerned, the maximum discrepancy of output voltage from the reference line is 0.084V. This results in linearity error being 2.5%. The Rogowski coil switch current sensor technique as well as phase current reconstruction could be equally applied to other technologies such as Si IGBT.

As far as the SC performance is concerned, fast detection time of 80 ns and reaction time of 200 ns are achieved, both of which limit overheating in the module. Besides that, soft turn-off limits excessive overshoots and puts them in the range below 300 V, even when ≈ 5 kA current was interrupted. Total time spent in protecting the short-circuit is around 1.2 μ s. The device did not reach breakdown energy and thermal runaway is avoided. Moreover, RSCS protection mechanism also does not interfere with the switching and conduction characteristics, it is responsive for all SC types, and has high noise immunity since it can operate in severe dv/dt environment without causing any problems.

VI. ACKNOWLEDGEMENT

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